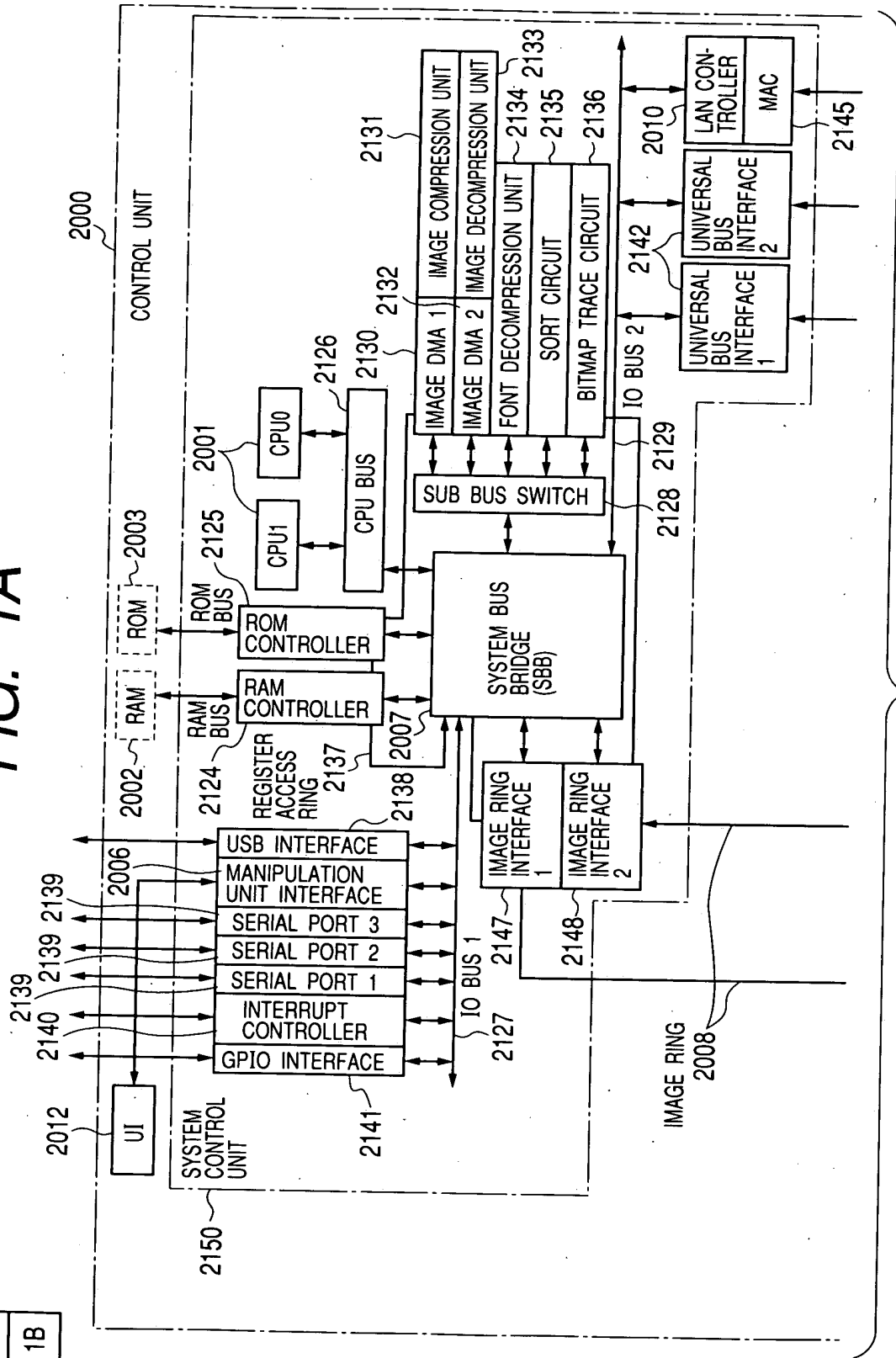


FIG. 1

FIG. 1A
FIG. 1B

FIG. 1A



TO FIG. 1B

FIG. 1B

FROM FIG. 1A

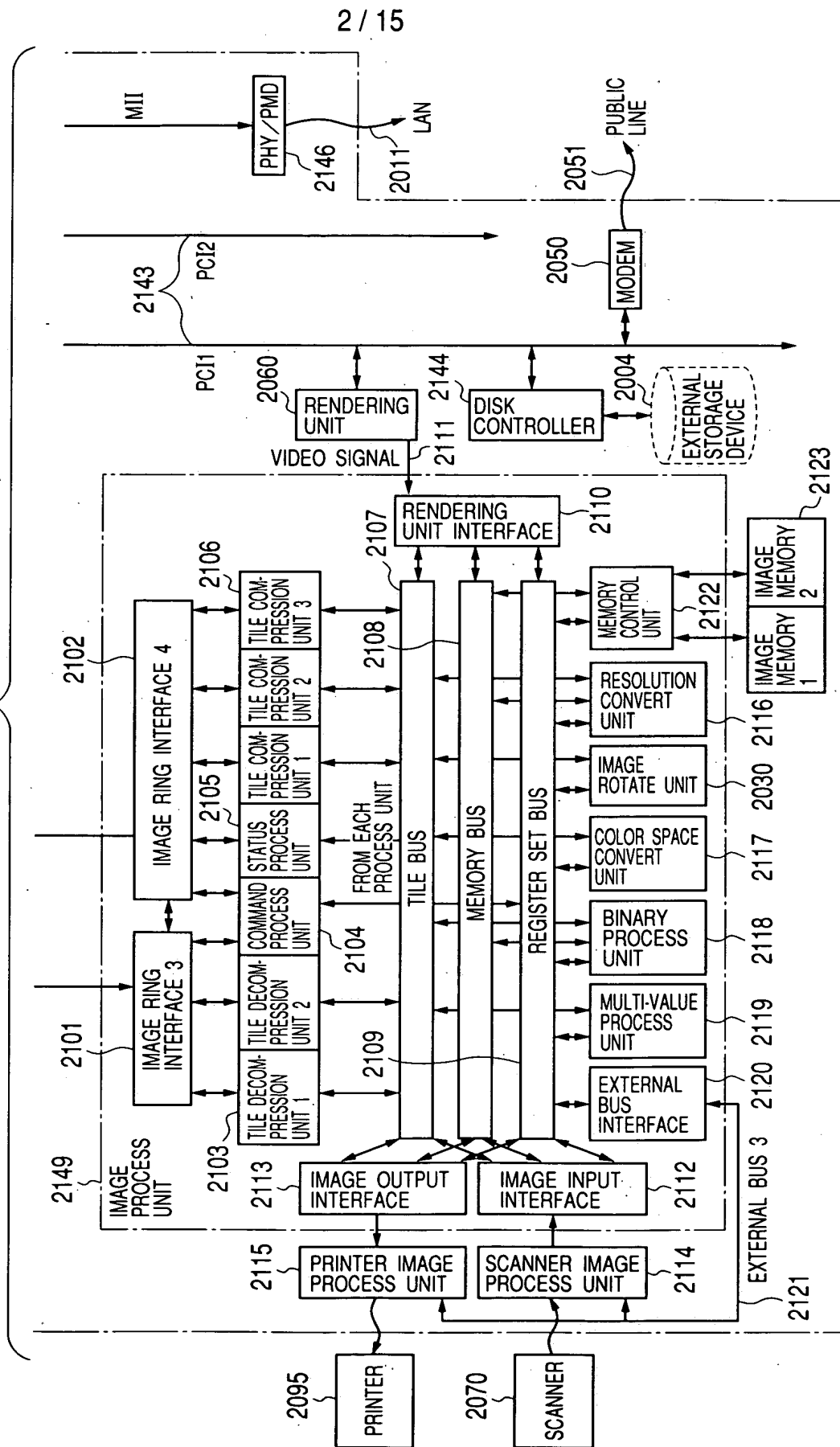


FIG. 2

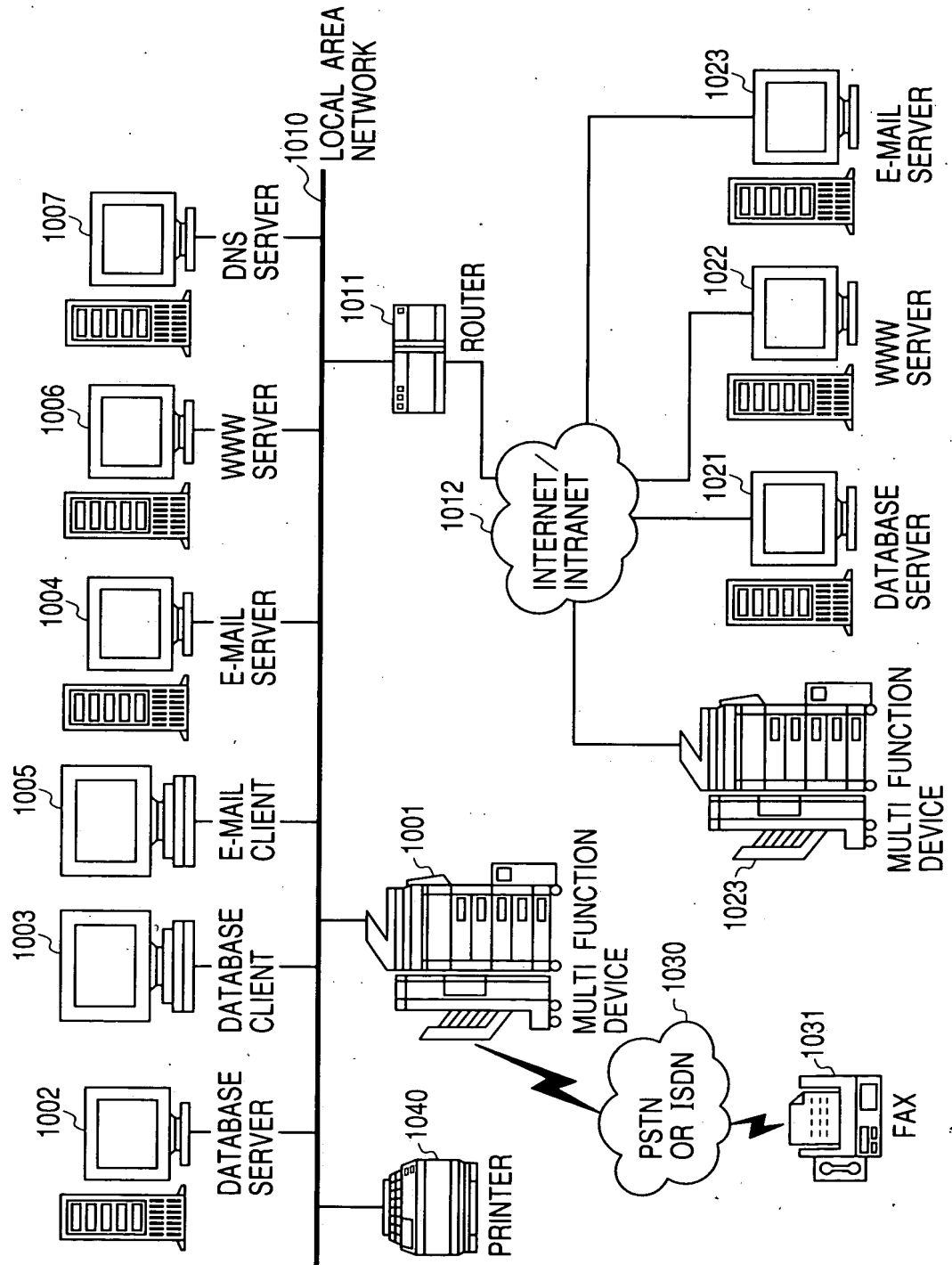
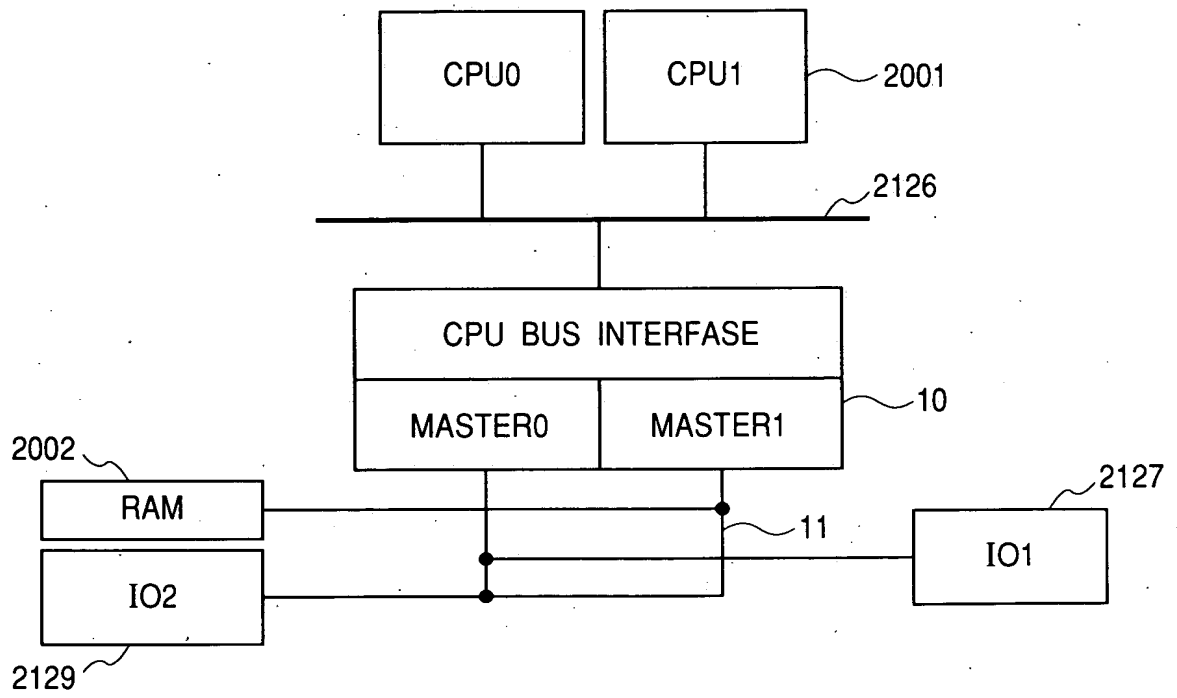


FIG. 3

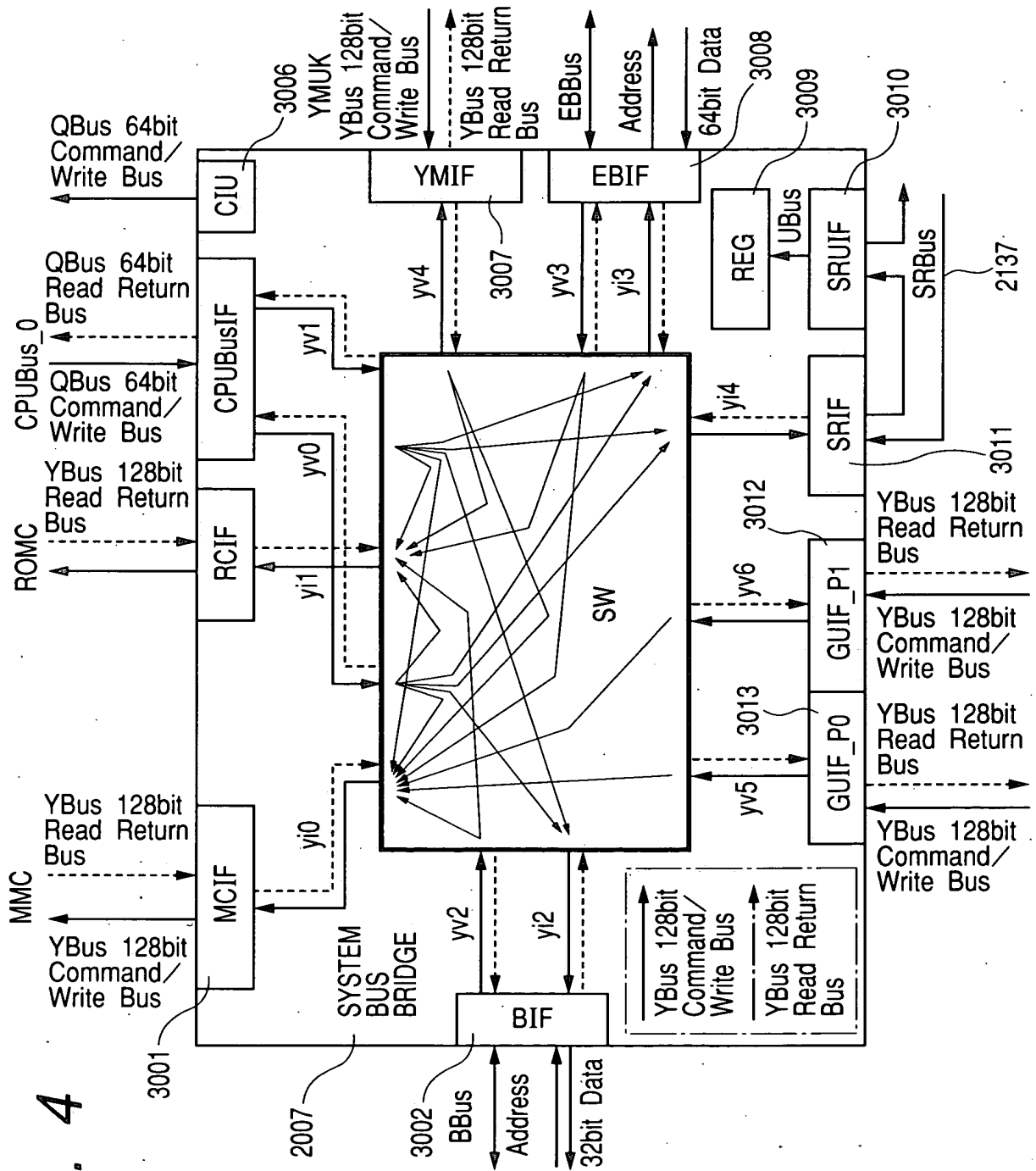
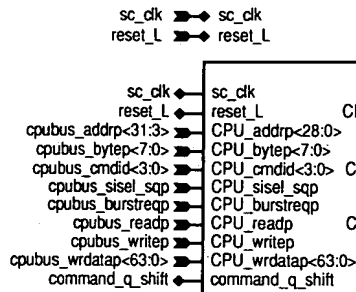


FIG. 5

FIG. 5A



101

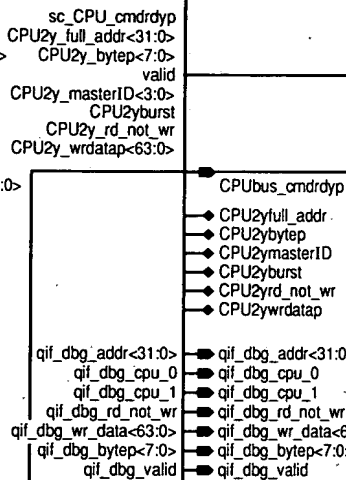
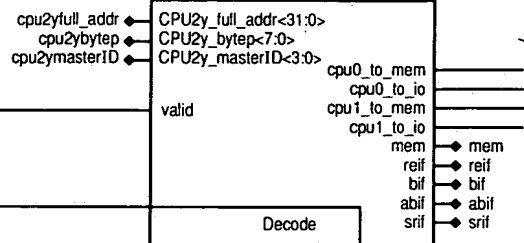
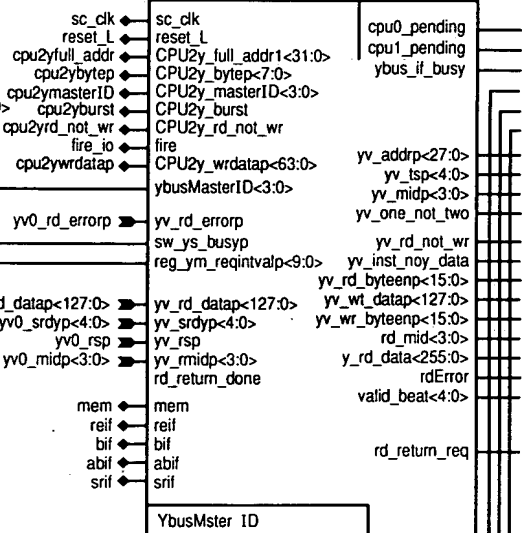


FIG. 5A

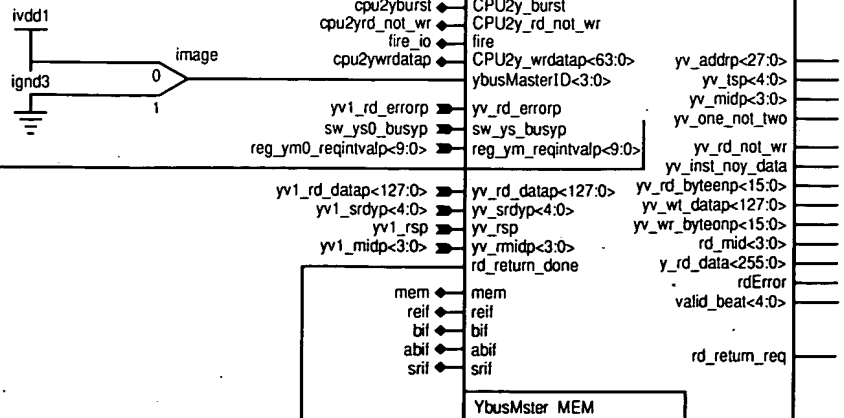
102



104



105



TO FIG. 5B

FIG. 5B

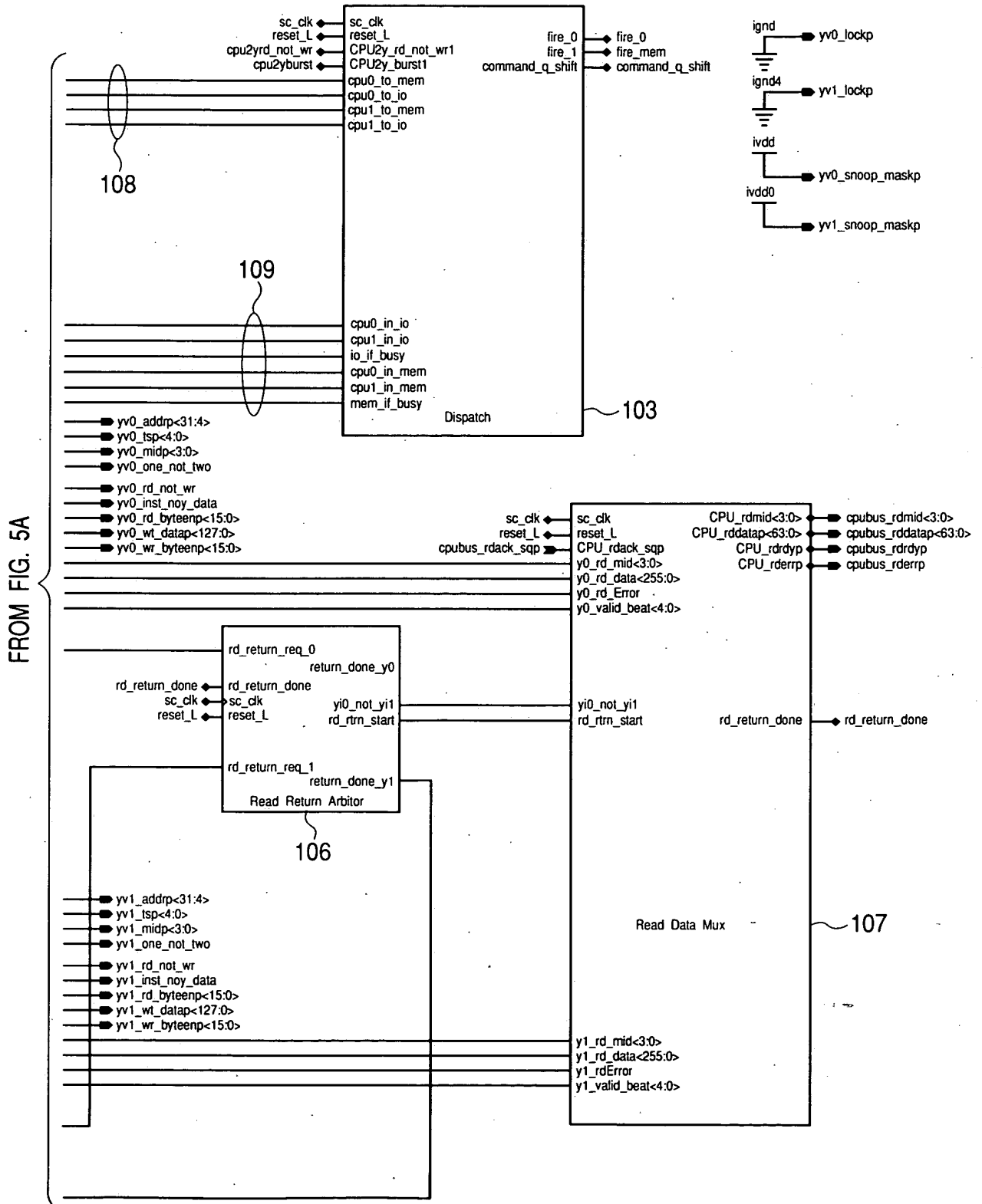


FIG. 6

Transaction Type	Description	
Non-cached Instruction Read	Single read	
cached Instruction Read	4 beat burst read	Critical word first (CWF)
Non-cached Load Data Read	Single read	
cached Load Data Read	4 beat burst read	CWF
Store Data Write	Single write	
Store Data Write Burst	4 beat burst write	CWF

FIG. 7

LAST SOURCE	LAST TARGET	CURRENT SOURCE	CURRENT TARGET	ISSUE PERMISSION
CPU0	IO A	CPU0	IO A	○
CPU0	IO A	CPU0	OTHER THAN IO A	×
CPU0	IO A	CPU0	MEM	×
CPU0	IO A	CPU1	IO A	○
CPU0	IO A	CPU1	OTHER THAN IO A	×
CPU0	IO A	CPU1	MEM	○
CPU0	MEM	CPU0	IO	×
CPU0	MEM	CPU0	MEM	○
CPU0	MEM	CPU1	IO	○
CPU0	MEM	CPU1	MEM	○
CPU1 (INVERSE AS WELL)				

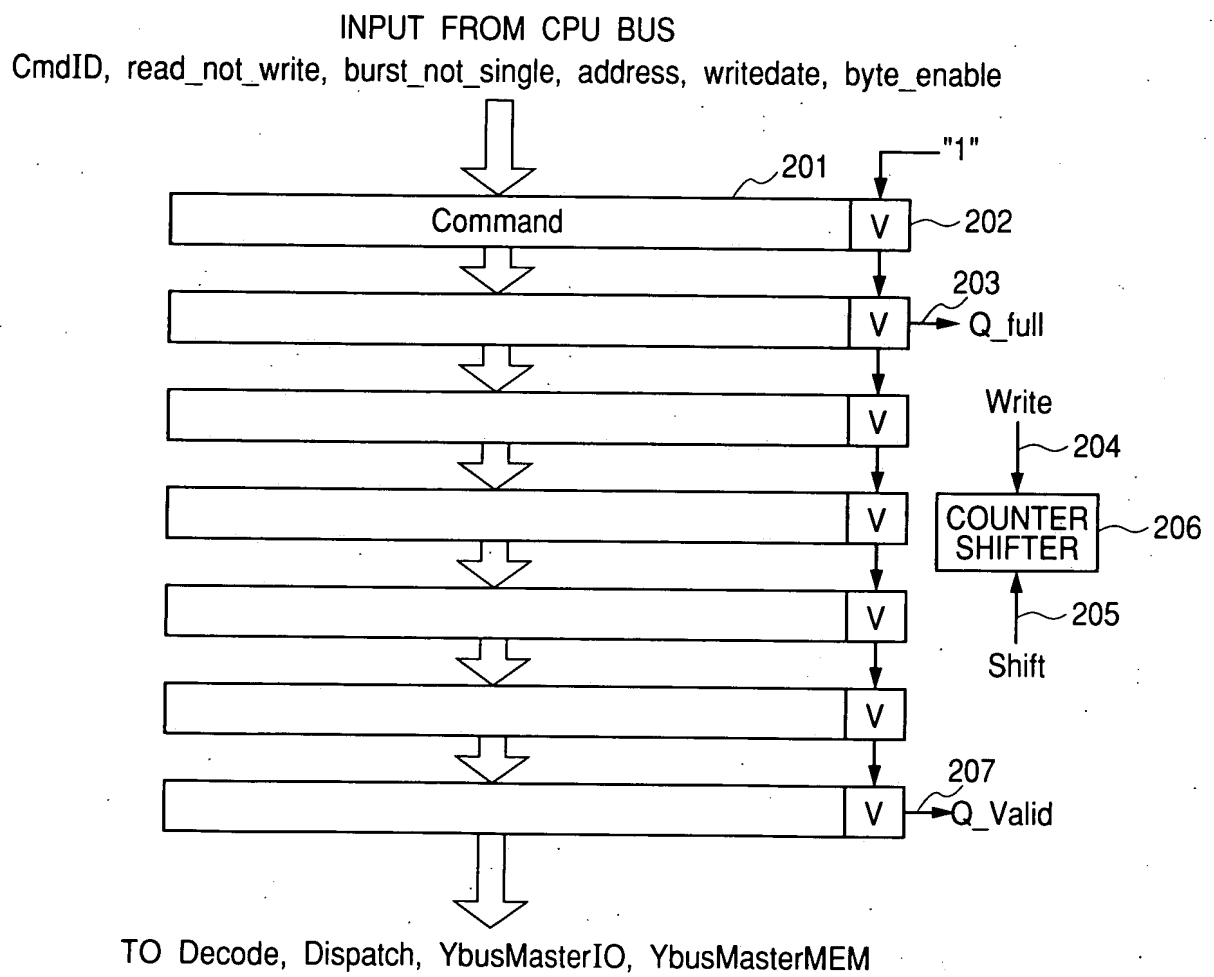
FIG. 8

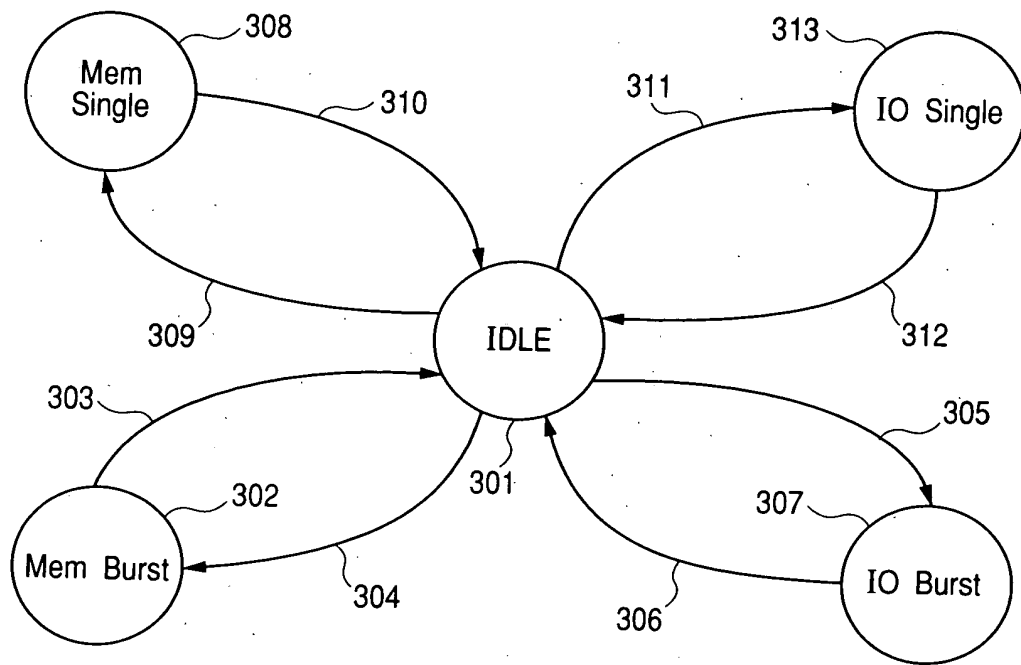
FIG. 9

FIG. 10

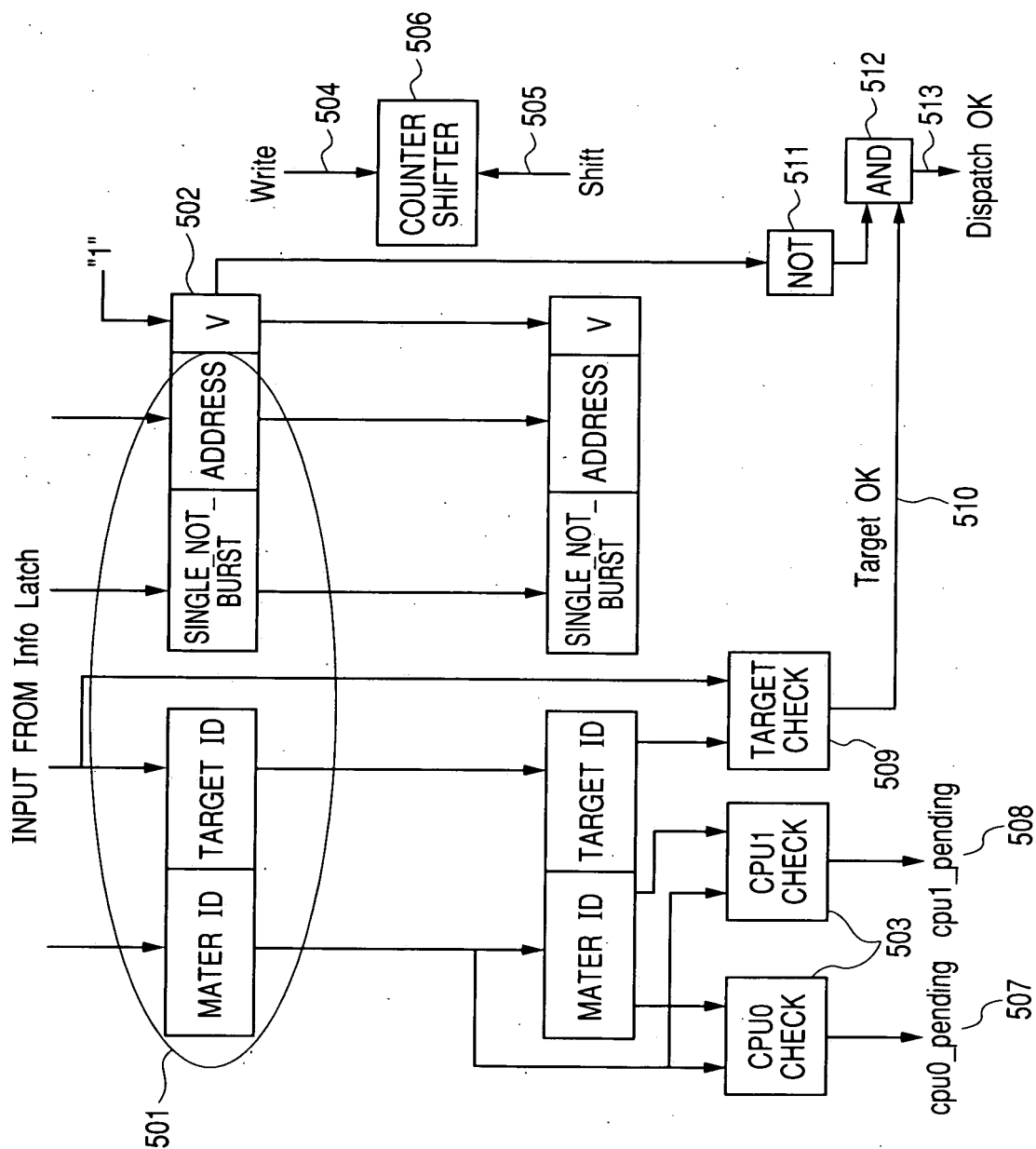


FIG. 11

FIG. 11A

FIG. 11B

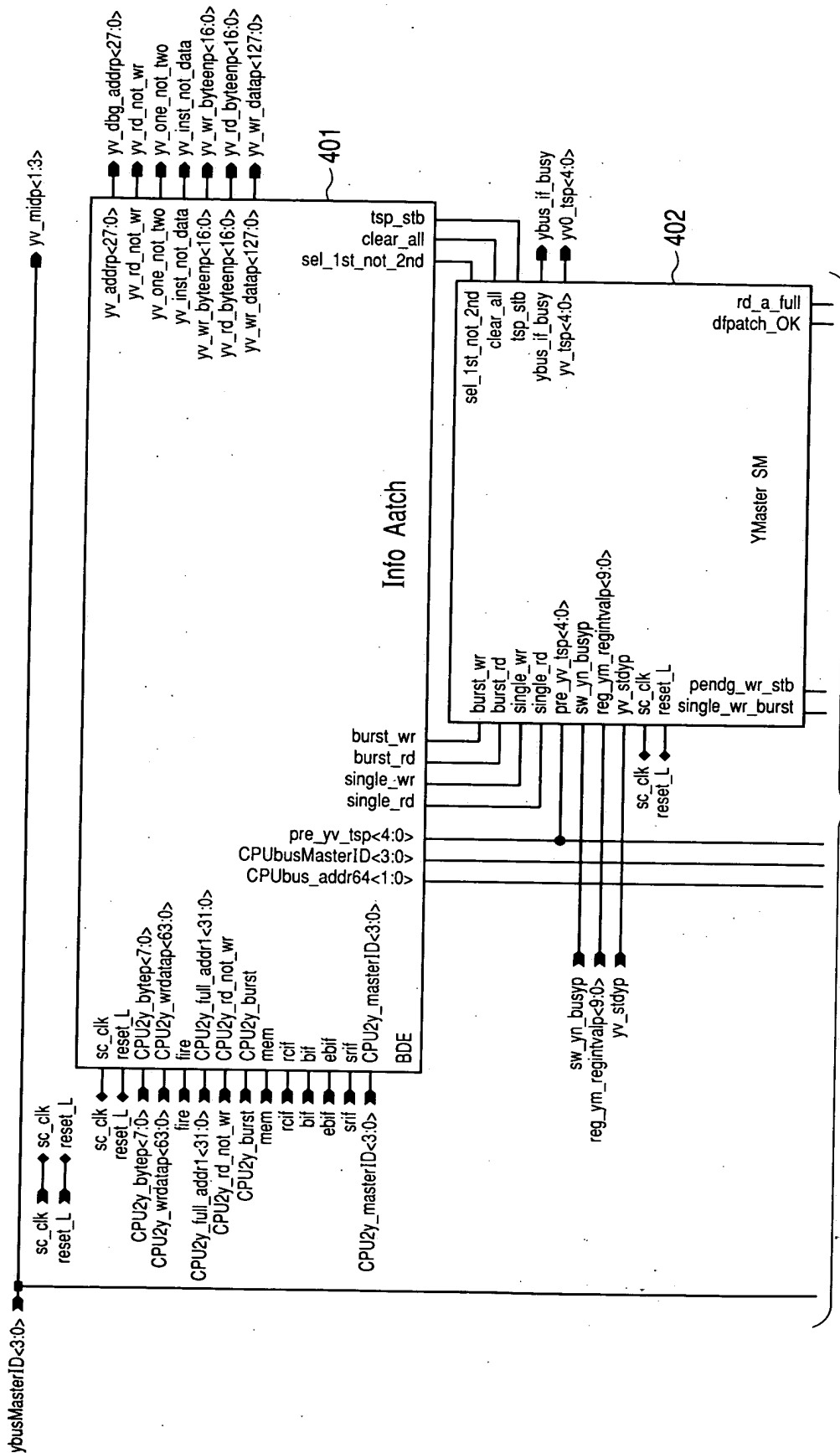


FIG. 11B

FROM FIG. 11A

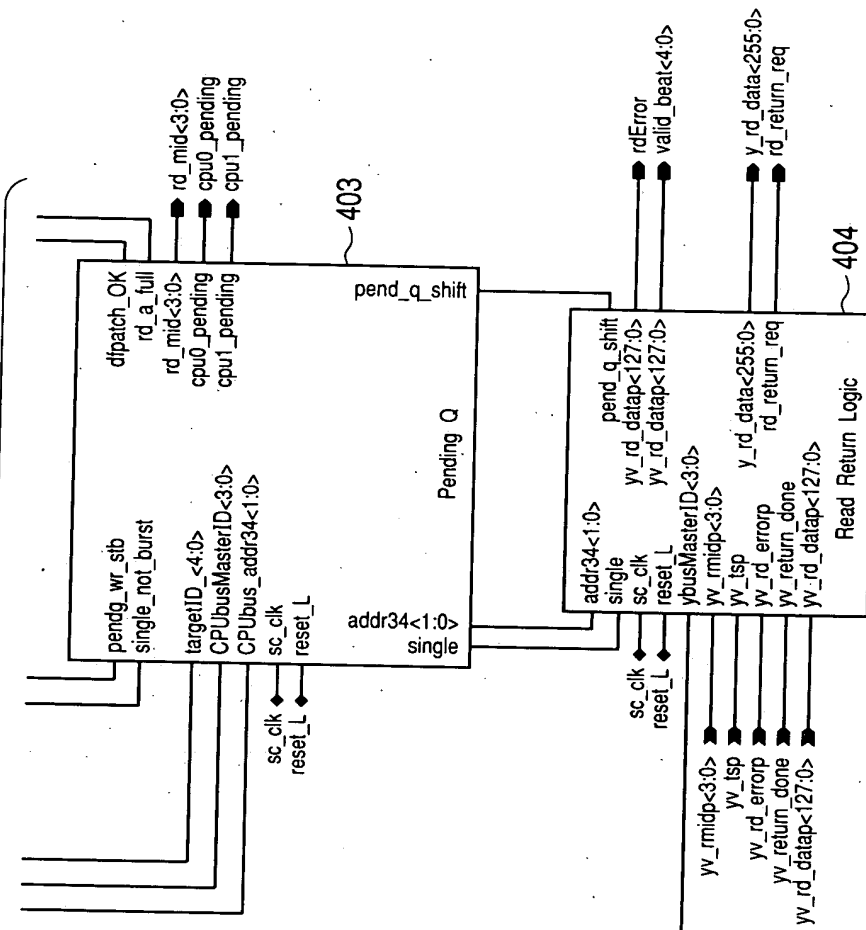


FIG. 12
PRIOR ART

